Attorney's Docket No.:10559-391001/P10256 - ADI APD1812-1-US

## REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim amendments are presented herein to obviate the current rejection. No new matter has been added.

### 35 USC §103

Claims 1-18, and 20-27 stand rejected under 35 USC §103(a) as allegedly being unpatentable over Atkins in view of Scales. Claim 19 stands rejected under 35 USC §103(a) as allegedly being unpatentable over Atkins in view of Scales and Tran. Claims 28-30 stand rejected under 35 USC §103(a) as allegedly being unpatentable over Atkins. These rejections are respectfully traversed.

Claim 1 recites "piping a second of said loop conditions from said first pipeline of the pipelined processor to a second pipeline of the pipelined processor" (for support, see, inter alia, specification page 11, line 22 to page 12, line 3). Claim 13 recites "pipe a loop setup instruction from the first pipeline to the second arithmetic unit in the second pipeline". Claim 26 recites "pipe a loop setup instruction from the first pipeline to a second arithmetic unit in the second pipeline".

Atkins has been cited as allegedly teaching defining loop conditions corresponding to a particular instance of a loop setup instruction for a first hardware loop and first propagating a first of said loop conditions of said first hardware loop via a first pipeline of a pipelined processor. Scales has been cited as allegedly teaching propagating loop conditions in parallel.

Scales describes a multiple execution unit microprocessor that includes an instruction pipeline, a loop cache memory in communication with the instruction pipeline, and a loop cache controller in communication with both the instruction pipeline and the loop cache memory (see, inter alia, Scales col. 11, lines 56-64). The instruction loop cache memory stores and retrieves up to N cycles of execution unit instructions for each execution unit (see, inter alia, Scales col. 11, lines 64-67). The loop cache memory issues new instructions to the execution units from the instruction pipeline and from the loop cache memory (see, inter alia, Scales col. 11, line 67 to col. 12, line 3). With this arrangement, instructions dispatched from a dispatch unit to a decode unit are simultaneously stored in loop cache memory (see, inter alia, Scales col. 12, lines 6 to 9). In parallel, additional instructions are issued in parallel from the loop cache memory to the decode units so that the hardware pipeline executes the new instructions and the loop cache instructions simultaneously (see, inter alia, Scales col. 12, lines 9 to 18).

There is no suggestion from the hypothetical combination of Atkins and scales that either of the new instructions or the loop cache instructions are piped from one pipeline to another. Rather, the new instructions are dispatched from the decode unit and from the loop cache memory in parallel for execution by the hardware pipeline. Therefore, the instructions are dispatched to the respective pipelines as opposed to being piped from one pipeline to another.

Accordingly, claims 1, 13, 26, and their respective dependent claims should be allowable.

Claim 7 recites "beginning to calculate said parameters using said first hardware loop, based on said loop conditions, prior to said propagating of said loop conditions in each of the

first and second pipelines to the hardware registers". Claim 22 recites "begin calculating data using said first hardware loop, prior to propagating the at least one loop condition of a particular instance of execution of said first hardware loop in the first pipeline to the set of registers and prior to propagating the at least one loop condition of the particular instance of execution of said first hardware loop in the second pipeline to the set of registers". Claim 28 recites "begin calculating data using said first hardware loop prior to propagation of the at least one of the loop conditions of said first hardware loop in the first pipeline to the second set of registers and prior to propagation of the at least one of the loop conditions of said first hardware loop in the second pipeline to the second set of registers".

Claims 7, 22, and 28 stand rejected based, in part, on a broad interpretation of the term 'propagating'. Each of claims 7, 22, and 28 have been amended to clarify that the propagating relates to the propagation of loop conditions in a pipeline to a register. Neither of Atkins or Scales disclose or suggest such an arrangement. Atkins describes an arrangement that loads incremented contents of an instruction register into a TOP register when a SETLOOP instruction is decoded (see, inter alia, Atkins col. 10, lines 17-20). Therefore, with Atkins, calculations occur only after a SETLOOP instruction has been decoded. Moreover, with regard to claims 22 and 28, there is no suggestion in Scales to begin calculations prior to propagate loop conditions to registers.

Accordingly, claims 7, 22, 28, and their respective dependent claims should be allowable.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Additionally, consideration of the Information Disclosure Statement filed on April 20, 2005 is earnestly solicited along with a copy of the form PTO-1449 with the Examiner's initials in the left column per MPEP 609.

Applicant asks that all claims be allowed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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